# MGZ18N65

650V GaN FET Enhancement Mode

Features

- 650V, 13A, $R_{DS(on)}$(typ.) = 150mΩ@VGS = 10V.
- Very low Q_{RR}
- Reduced Crossover Loss
- Easy to drive with commonly-used gate drivers
- Enables AC-DC bridgeless totem-pole PFC designs
  - Increased power density
  - Reduced system size and weight
  - Overall lower system cost
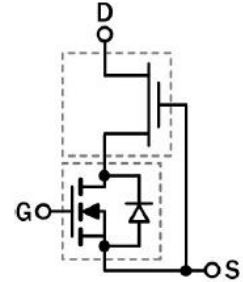- Achieves increased efficiency in both hard- and soft switched circuits
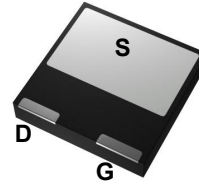
Application

- Power adapters
- Low power SMPS
- Lighting

DFN8X8-3L
Bottom View
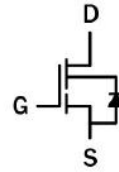
Cascode Schematic Symbol

Cascode Device Structure

Absolute Maximum Ratings （Tc = 25°C unless otherwise noted）

Symbol	Parameter		Limit	Unit
V_{DS}	Drain-Source Voltage		650	V
$V_{(TR)DSS}$	Transient Drain to Source Voltage [a]		800	V
V_{GSS}	Gate-Source Voltage		± 20	V
P_D	Maximum power Dissipation @T_C = 25°C		52	W
I_D	Drain Current-Continuous	T_C = 25°C [b]	13	A
	Drain Current-Continuous	T_C = 100°C [b]	8.4	A
I_{DM}	Drain Current-Pulsed	Pulse Width = 10μs	60	A
T_C	Operating Temperature Case		-55 to +150	°C
T_J	Operating Temperature Junction		-55 to +150	°C
T_S	Storage Temperature		-55 to +150	°C
T_{SOLD}	Soldering Peak Temperature [c]		260	°C

Thermal Characteristics

Symbol	Parameter	Typical	Unit
$R_{θJC}$	Thermal Resistance Junction-Case	2.4	°C/W
$R_{θJA}$	Thermal Resistance Junction-Ambient [d]	50	°C/W

Electrical Characteristics（ T_J = 25°C unless otherwise noted）

■ Off Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{(BL)DSS}$	Reverse Breakdown Voltage	V_{GS} = 0V	650	-	-	V
I_{DSS}	Reverse Leakage Current	V_{GS} = 0V, V_{DS} = 650V T_J = 25°C	-	2.5	25	µA
		V_{GS} = 0V, V_{DS} = 650V T_J = 150°C	-	10	-	µA
I_{GSS}	Gate-to-source Leakage Current	V_{DS} = 0V, V_{GS} = ±20V	-	-	±100	nA

■ On Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D =500µA	3.3	4.0	4.8	V
$R_{DS(on)eff}$	On Resistance	V_{GS} = 10V, I_D =8.5A T_J = 25°C	-	150	180	mΩ
		V_{GS} = 10V, I_D =8.5A T_J = 150°C	-	307	-	

■ Dynamic Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 400 V f=1MHz	-	598	-	pF
C_{OSS}	Output Capacitance		-	30	-	
C_{RSS}	Transfer Capacitance		-	1	-	
$C_{o(er)}$	Output Capacitance, energy related	V_{GS} = 0 V, V_{DS} = 0~400 V	-	43	-	pF
$C_{o(tr)}$	Output Capacitance, time related		-	85	-	

■ On Characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{GS} = 0~12 V, V_{DS} = 400 V , I_D = 10 A , Rg = 70 Ω	-	13	-	ns
t_r	Turn-On Rise Time		-	25	-	
$t_{d(off)}$	Turn-Off Delay Time		-	47	-	
t_f	Turn-Off Fall Time		-	34	-	
Q_G	Total Gate Charge	V_{GS} = 0~10 V, V_{DS} = 400 V , I_D = 8.5 A	-	8.0	-	nC
Q_{GS}	Gate-Source Charge		-	3.3	-	
Q_{GD}	Gate-Drain Charge		-	2.0	-	
Q_{OSS}	Output Charge	V_{GS}=0V,V_{DS}=0~400 V	-	34	-	nC

■ **Drain-Source Diode Characteristics**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
I_S	Reverse Current	$V_{GS} = 0$ V	-	-	13	A
V_{SD}	Reverse Voltage	$V_{GS} = 0V$, $I_S = 10$ A	-	2.4	-	V
		$V_{GS} = 0V$, $I_S = 5$ A	-	1.6	-	V
t_{RR}	Reverse Recovery Time	$I_S = 10$ A ,$V_{DS}= 400V$, di/dt = 1000 A/µs	-	31	-	ns
Q_{RR}	Reverse Recovery Charge		-	40	-	nC

Notes:

a. In off-state, spike duty cycle D<0.01, spike duration <1µs .

b. For increased stability at high current operation.

c. Reflow MSL3 .

d. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70µm thickness).

■ **DFN8X8-3L Package Information**

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	2.20	2.25	2.30
c	0.20 REF.		
D	7.90	8.00	8.10
D2	6.85	7.00	7.15
E	7.90	8.00	8.10
E2	4.03	4.18	4.33
e	4.75 BSC		
K	2.50	---	---
L	0.70	0.80	0.90
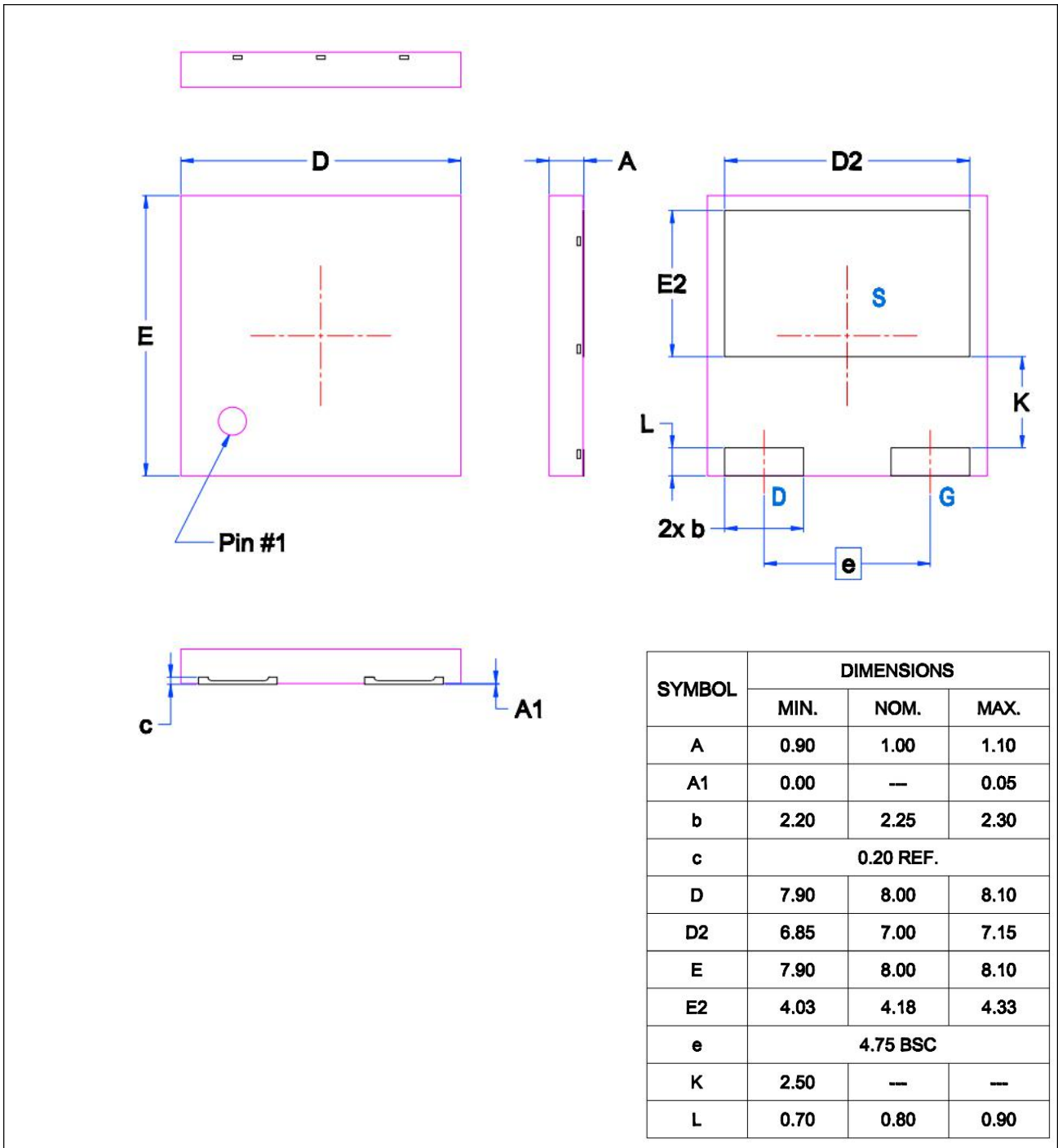
■ **Revision History**

Version	Date	Subjects (major changes since last revision)
0.1	2021-12-10	Preliminary Version